

REMARKS

Reconsideration is respectfully requested.

Claim 1 has been amended to more clearly indicate the in-line electrical connection of the wiring unit between the data pad unit and the data line. No new matter has been added by these amendments.

With respect to the requirements for drawing amendments to Fig. 3A, attached hereto are drawing corrections to include the corrected identification of a data odd pad 17a and a data even pad 17b. New drawing FIG. 3A has been proposed to correct for the previously noted discrepancies in the odd and even data pads, for which the Examiner's approval is respectfully requested. A marked up drawing showing the corrections are also attached.

Applicants note the withdrawal of the indefiniteness rejection based on 35 U.S.C. § 112, second paragraph, with appreciation.

With respect to the prior art rejections, it is respectfully suggested that the Applicants Admitted Prior Art (AAPA), as shown in Figs. 1 and 2, fails to anticipate Claims 1-3, 5-7, and 9-11 in that each limitation recited in at least independent Claims 1, 5 and 9 is not taught or otherwise suggested by the AAPA, for the AAPA fails to show the limitation by which "the wiring unit for testing defects of the data line being connected between the data pad unit and the data line," (emphasis added). In contradistinction, and as set forth at page 2, lines 8-14 of the originally filed specification, (page 1, line 19 through page 2, line 2 of the substitute specification), the wiring 20 is formed "on the corner of the upper part of panel 10." However, and this is a significant point, no direct interconnection to the data line, gate line or common voltage line is shown. Thus, there is no interconnection specifically taught to the wiring 20, and certainly no connection between the data line and the data pad 17a or 17b, as is recited in, respectively, Claims 1, 5 and 9. It is respectfully suggested that the rejection of Claims 1-3, 5-7, and 9-11 is therefore improper.

It should be noted that several distinguishing features are present in the invention not shown by the AAPA. First, the wiring 20 in Fig. 2 denotes the wiring connected between the X-PCB and Y-PCB, in a FPCless type device. Each of the wiring 30a, 30b in Figs. 3A and 3B corresponds to the wiring 20 in Fig. 2. That is, each of the wiring 30a, 30b in Fig. 3 takes the place of the wiring 20 in Fig. 2, and is the wiring connected between the X-PCB and Y-PCB, in a FPCless type device.

The novel characteristic of the present invention is to connect one end of each of the wiring 30a, 30b to the data pad or the gate pad, and to connect the other end of each of the wiring 30a, 30b to the corresponding data line or gate line in order to test whether the wiring (30a, 30b) is disconnected or short. To accomplish this test, a test signal can be applied to the data pad or gate pad only, without requiring connection to the other pads, for example voltage pads, etc, that are required in the panels having the wiring 20 in the corner.

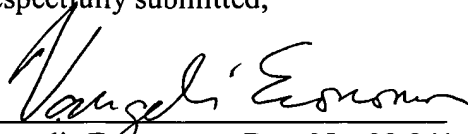
The AAPA also fails to show the wiring unit for testing defects of the data line or gate line which is connected in series between the data pad unit and the data line, as is recited in Claims 1, 5 and 9, or between the gate pad unit and the gate line, respectively. In addition, the feature of the present invention as claimed in Claim 4 is in not simply the zigzag shape of the wiring unit, but the existence of the wiring unit for testing defects of the data line or gate line, being formed in a zigzag shape in the specified portion of the circuit. Chung et al. merely discloses an LCD apparatus comprising stitch defect correcting elements included in the data lines or gate lines, to eliminate stitching defects caused by an irregularity in the width of a gate line or data line, and does not disclose or suggest any attempts to test defects that may be present in panel wiring in a FPC or PCB less module. Therefore, the present inventions as claimed in claims 1 to 12 are not anticipated by the AAPA nor made obvious over the AAPA in view of Chung et al.

Similarly, the rejection of Claims 4, 8 and 12 is also improper in that the combination of AAPA and Chung et al. fail to set forth a *prima facie* case of obviousness, because, as set forth above with respect to independent Claims 1, 5 and 9, the same recited limitation is not taught by either of the references, and thus is entirely missing from the proposed combination. Chung et al. fail to provide this missing element, and therefore it is not obvious to include the zigzag structure in the AAPA as suggested. Moreover, the incentive identified by Chung et al., to correct for the “stitching defect” is not relevant to the modification of the AAPA device simply because the “stitching defect” does not appear to be a consideration in the present invention or in the AAPA, which is directed to test for disconnection and short anomalies, as is set forth in the claims. It is not Applicants intent to import the specification statements set forth in the specification at page 10, lines 12-17. Applicant merely refers to these statements to further explain the meaning of the language recited in the claims. That is, the wiring pattern shape is formed in the inventive TFT array so that the wiring provides means for quick and easy determination of short or disconnection anomalies, as recited in Claims 1, 5 and 9, which can be used for testing integrity of the connections. This does not relate to any “stitching defect,” and as such, a teaching, suggestion or incentive to perform the modification as proposed in the rejection is lacking.

For the above reasons, it is considered that the claims, as amended, find support in the application specification as filed, and that the combination of elements recited in the pending claims, as amended, distinguish over the references of record. Accordingly, reconsideration and

withdrawal of the outstanding rejections are respectfully requested an indication of allowable subject matter is earnestly solicited.

Respectfully submitted,

A handwritten signature in black ink, appearing to read "Vangelis Economou", written over a horizontal line.

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